

Listing and Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1 1. (currently amended) A signal processing system comprising:
2 means for providing a first signal intrinsic to an integrated circuit;
3 means for providing a first operational function to the first signal, said function
4 being provided at a pin of the integrated circuit,
5 means for providing a second operational function to the first signal by the
6 integrated circuit to produce a third signal representative of the first signal at an output
7 of the second operational function providing means, and
8 means for coupling a second signal extrinsic of the integrated circuit to the pin of
9 the integrated circuit so that the means for providing the second operational function
10 operates on the second signal to produce a fourth signal representative of the second
11 signal at the output of the second operational function providing means.

1 2. (currently amended) The signal processing system ~~processor~~ of claim 1
2 wherein the first and second signals are analog audio signals.

1 3. (original) The signal processing system of claim 1 wherein the first operational
2 function is de-emphasis and the second operational function is a variable attenuator.

1 4. (original) The signal processing system of claim 1 wherein the second signal is
2 switchable "in" and "out", and when switched "in", the first signal is switched "off".

1 5. (original) The signal processing system of claim 1 wherein the pin serves as a
2 bi-directional conduit for signals.

1 6. (currently amended) A signal processing system comprising:
2 means for providing a first operational function to a first signal at a pin of an
3 integrated circuit, the first signal being intrinsic to the integrated circuit, and
4 means for coupling a second signal extrinsic of the integrated circuit to the pin of
5 the integrated circuit so that a means within the integrated circuit for providing a second
6 operational function operates on the second signal, wherein
7 the second signal is switched "in" and "out" at the pin, and when the second signal is
8 switched "in", the first signal is disabled at the pin.

1 7. (currently amended) The signal processing system processor of claim 6
2 wherein the first and second signals are analog audio signals.

1 8. (original) The signal processing system of claim 6 wherein the first operational
2 function is de-emphasis and the second operational function is a variable attenuator.

1 9. (cancelled)

1 10. (original) The signal processing system of claim 6 wherein the pin serves as
2 a bi-directional conduit for signals.

1 11. (original) A signal processing system comprising:
2 means for providing an operational function to a first signal at a pin of an
3 integrated circuit, the first signal being intrinsic to the integrated circuit, and
4 means for coupling a second signal extrinsic of the integrated circuit to the pin of
5 the integrated circuit,

the coupling of the second signal to the pin switching "off" the presence of the first signal at the pin.

12. (currently amended) The signal processing system ~~processor~~ of claim 11 wherein the first and second signals are analog audio signals.

13. (original) The signal processing system of claim 11 wherein the first operational function is de-emphasis.

14. (original) The signal processing system of claim 11 wherein the pin serves as a bi-directional conduit for signals.

15. (original) A signal processing system comprising:
means for providing a first signal intrinsic to an integrated circuit;
means for providing a first operational function to the first signal at a pin of the integrated circuit,

means for providing a second operational function to the first signal by the integrated circuit, and

means for coupling a second signal extrinsic of the integrated circuit to the pin of the integrated circuit so that the means for providing the second operational function operates on the second signal,

the second signal being switchable "in" and "out", and when switched "in" the first signal is switched "off" at the pin.

16. (original) The signal processing system of claim 15 wherein the pin serves as a bi-directional conduit for signals.

17. (currently amended) The A signal processing system of claim 15 wherein comprising:

3 ~~_____ means for providing a first signal intrinsic to an integrated circuit;~~

4 ~~_____ means for providing a first operational function to the first signal at a pin of the~~
5 ~~integrated circuit,~~

6 ~~_____ means for providing a second operational function for the first signal by the~~
7 ~~integrated circuit, and~~

8 ~~_____ means for coupling a second signal extrinsic of the integrated circuit at the pin so~~
9 ~~that the means for providing the second operational function operates on the second~~
10 ~~signal,~~

11 the pin serves ~~serving~~ as a bi-directional conduit for signals,

12 ~~the second signal being switchable "in" and "out", and when switched "in", the first~~
13 ~~signal is switched "off" at the pin.~~

1 18. (currently amended) A circuit for switchably coupling a signal comprising:

2 first and second transistors each having respective base/gate electrode,
3 emitter/source and collector/drain electrodes, the two transistors being of the same
4 conductivity type and connected in series between a voltage supply and a reference
5 point,

6 in a signal coupling mode, the signal output coupling being from the first
7 emitter/source electrode, the second collector/drain electrode being coupled to the first
8 emitter/source electrode through a resistor, the first emitter/source electrode being at a
9 first impedance with respect to the reference point and

10 the first base/gate having bias means and receiving the input signal with the bias
11 means placing the first transistor in a linear signal transmission state, and the output

12 signal being coupled out by the first emitter/source, the bias means also biasing the
13 second base/gate electrode so that the second transistor is in a saturated state,
14 the circuit being switchable from the signal coupling mode to a non-signal
15 coupling mode by the bias means placing the first transistor in a cutoff state so that the
16 first transistor is rendered non-coupling for the signal, the bias means also placing the
17 second transistor in a cutoff state so that via action of the second collector/drain
18 electrode, the first emitter/source electrode is switched to be at a second high
19 impedance higher than the first impedance with respect to the reference point thus
20 removing impedance loading by the first emitter/source electrode.